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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,344	08/28/2003	Sung-Yung Lee	5649-1162	6659

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EXAMINER	
QUINTO, KEVIN V	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/650,344	LEE ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,5-20,33-38,44 and 45* is/are allowed.

6)☒ Claim(s) *21-32 and 39-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-3 and 5-45 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 21-32 and 39-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Xing et al. (USPN 6,090,697).

4. In reference to claim 21, Xing et al. (USPN 6,090,697, hereinafter referred to as the "Xing" reference) discloses a similar capacitor. Figure 5 of Xing discloses an MIM capacitor with an upper electrode (not labeled), a lower electrode (504), and a dielectric film (not labeled) which is interposed between them. The lower electrode (504) has a bottom and a sidewall. The bottom of the lower electrode (504) is disposed over an oxidation barrier pattern which defines a lower electrode platform with a top surface. The oxidation barrier pattern resides above and is in electrical communication with a region of a semiconductor substrate (not shown). The bottom of the lower electrode (504) has a surface area that is substantially coextensive with the surface area of the

top surface area of the platform defined by the oxidation barrier pattern. The dielectric layer is oriented in a substantially straight line that conforms to the external perimeter shape of the sidewall of the lower electrode (504) and an adjacent underlying sidewall of the oxidation barrier pattern lower electrode platform.

5. With regard to claim 22, the dielectric film is made of BST or barium strontium titanate (column 5, lines 35-52). BST has a higher dielectric constant than ONO or oxide-nitride-oxide (see Huang, USPN 6,353,269 B1, column 6, lines 38-40), thus meeting the claim.

6. In reference to claim 23, the device of figure 5 resides in a unit cell of an integrated circuit DRAM memory device (column 3, lines 29-31).

7. In reference to claims 24 and 25, the device is in a unit cell of a DRAM memory device (column 3, lines 29-31). The dielectric film of the unit cell is made of BST or barium strontium titanate, a known ferroelectric substance (see Leung et al., USPN 5,563,762, column 1, lines 46-50); thus forming a ferroelectric memory device.

8. In reference to claim 26, Xing (USPN 6,090,697) discloses a similar semiconductor device. Figure 5 of Xing discloses a semiconductor device with a capacitor. It is understood that there is a plurality of metal-insulator-metal capacitors. Each capacitor has an upper electrode (not labeled), a lower electrode (504), and a dielectric film (not labeled) which is interposed between them. The capacitors reside above a semiconductor substrate (not shown). Each capacitor has an oxidation barrier pattern (not labeled) which is in electrical communication with respective regions of a semiconductor substrate. The lower electrode (504) of each capacitor has a bottom

surface area which is substantially equal to the surface area of the upper surface of the underlying oxidation barrier pattern. The dielectric layer has a substantially vertical configuration about the sidewalls of the lower electrodes.

9. In reference to claim 27, Xing (USPN 6,090,697) discloses a similar semiconductor device. Figure 5 of Xing discloses a semiconductor device with a capacitor. It is understood that there is a plurality of metal-insulator-metal capacitors. Each capacitor has an upper electrode (not labeled), a lower electrode (504), and a dielectric film (not labeled) which is interposed between them. The capacitors reside above a semiconductor substrate (not shown). Each capacitor has an oxidation barrier pattern (not labeled) which is in electrical communication with respective regions of a semiconductor substrate. The lower electrode (504) of each capacitor has a bottom surface area which is substantially equal to the surface area of the upper surface of the underlying oxidation barrier pattern. The dielectric layer has a substantially vertical configuration about the sidewalls of the lower electrodes. The lower electrode is substantially cylindrical with a closed continuous surface bottom.

10. With regard to claim 28, the dielectric film is made of BST or barium strontium titanate (column 5, lines 35-52). BST has a higher dielectric constant than ONO or oxide-nitride-oxide (see Huang, USPN 6,353,269 B1, column 6, lines 38-40), thus meeting the claim.

11. In reference to claim 29, the capacitor of figure 12 defines a part of a unit cell of an integrated circuit DRAM memory device (column 3, lines 29-31).

12. In reference to claims 30 and 31, the capacitor defines a part of a unit cell of a DRAM memory device (column 3, lines 29-31). The dielectric film of the unit cell is made of BST or barium strontium titanate, a known ferroelectric substance (see Leung et al., USPN 5,563,762, column 1, lines 46-50); thus forming a ferroelectric memory unit cell.

13. With regard to claim 32, Xing (USPN 6,090,697) discloses a similar fabrication method. Figure 5 of Xing discloses a plurality of MIM capacitors in unit cells of an integrated circuit memory device. An oxidation barrier pattern (not labeled) is formed on a semiconductor substrate (not shown). A lower electrode (504) is disposed on the oxidation barrier pattern so that a top surface area of the oxidation barrier pattern is substantially equal to a bottom surface are of the lower electrode (504). A dielectric layer (not labeled) is formed over the sidewalls of the lower electrode and oxidation barrier pattern in a substantially vertical orientation.

14. In reference to claim 39, the lower electrode is substantially cylindrical with a closed continuous surface bottom that resides on the oxidation barrier pattern.

15. In reference to claim 40, figure 5 of Xing shows that the lower electrode (504) comprises two substantially spaced apart upwardly extending sidewalls with an upper portion and a closed bottom surface. The closed bottom surface resides on the oxidation barrier lower electrode platform.

16. In reference to claim 41, the lower electrode is substantially cylindrical with a closed continuous surface bottom that resides on the oxidation barrier pattern.

17. In reference to claim 42, the lower electrode is substantially cylindrical with a closed continuous surface bottom that resides on the oxidation barrier pattern.

18. In reference to claim 43, figure 5 of Xing shows that the lower electrode (504) comprises two substantially spaced apart upwardly extending sidewalls with an upper portion and a closed bottom surface. The closed bottom surface resides on the oxidation barrier lower electrode platform.

Allowable Subject Matter

19. Claims 1-3, 5-20, 33-38, 44, and 45 are allowed.

20. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests a fabrication method for a semiconductor device with a metal insulator metal capacitor containing a stack with a oxidation barrier pattern and a capping layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

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